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Description

[STRUCTURE AND METHOD FOR LOCAL RESISTOR ELEMENT IN INTEGRATED CIRCUIT TECHNOLOGY]

BACKGROUND OF INVENTION

[0001] FIELD OF THE INVENTION

[0002] This invention relates generally to localized resistor elements in semiconductor components and, in particular, to protection from failures and errors caused by unwanted electrical events.

[0003] BACKGROUND OF THE INVENTION

[0004] The utilization of resistors is important in semiconductor circuitry design to isolate single components, circuits, sub-circuits, and functional design blocks. In single components, resistors are used to provide improvements in the reliability aspects of semiconductor circuits. Resistor element incorporation is an important reliability mechanism to provide electrostatic discharge protection (ESD)

and to prevent CMOS "latchup", electrical overstress (EOS), hot electron and other soft error rate (SER) events. Resistors are also used to prevent parasitic interaction between circuits.As electronic components are getting smaller and smaller along with the internal structures in integrated circuits, it is getting easier to either completely destroy or otherwise impair electronic components through electrical events. In particular, many integrated circuits are highly susceptible to damage from the discharge of static electricity, even at levels which can neither be seen nor felt. Electrostatic discharge (ESD) is the transfer of an electrostatic charge between bodies at different electrostatic potentials (voltages), caused by direct contact or induced by an electrostatic field. The discharge of static electricity, or ESD, has become a critical problem for the electronics industry. Device failures are not always immediately catastrophic. Often, the device is only slightly weakened but is less able to withstand normal operating stresses and, hence, may result in a reliability problem. Therefore, various ESD protection circuits must be included in the device to protect the various components. Many considerations are necessary for ESD protection circuits.

[0005] Latchup is known to occur from single event upsets (SEU),

also referred to as soft error (SER) events. Single event upsets can include terrestrial emissions from nuclear processes and cosmic ray events, as well as events in space environments. Cosmic ray particles can include proton, and neutron, gamma events, as well as a number of particles that enter the earth atmosphere. Terrestrial emissions from radioactive events, such as alpha particles, and other radioactive decay emissions can also lead to latchup in semiconductors.

[0006] Latchup occurs when a pnpn structure transitions from a low-current/high-voltage state to a high-current/low-voltage state through a negative resistance region (i.e. forming an S-Type I-V (current/voltage) characteristic). Latchup is typically understood as occurring within a pnpn structure, or silicon controlled rectifier (SCR) structure. Interestingly enough, these pnpn structures can be intentionally designed, or even unintentionally formed between structures. Hence, latchup conditions can occur within peripheral circuits or internal circuits, within one circuit (intra-circuit) or between multiple circuits (inter-circuit).

[0007] Latchup is typically initiated by an equivalent circuit of a cross-coupled pnp and npn transistor. With the base and

collector regions being cross-coupled, current flows from one device leading to the initiation of the second ("regenerative feedback"). These pnp and npn elements can be any diffusions or implanted regions of other circuit elements (e.g., P-channel MOSFETs, N-Channel MOSFETs, resistors, etc.) or actual pnp and npn bipolar transistors. In CMOS, the pnpn structure can be formed with a p-diffusion in an n-well, and an n-diffusion in a p-substrate (parasitic pnpn); in this case, the well and substrate regions are inherently involved in the latchup current exchange between regions.

[0008] Latchup can be initiated from internal or external stimulus. The condition for triggering a latchup is a function of the current gain of the pnp and npn transistors, and the resistance between the emitter and the base regions. This inherently involves the well and substrate regions. The likelihood or sensitivity of a particular pnpn structure to latchup is a function of spacings (e.g. base width of the npn and base width of the pnp), current gain of the transistors, substrate resistance and spacings, the well resistance and spacings, and isolation regions.

[0009] Static random access memory cells or circuits are widely known in the semiconductor technology. A schematic of a

typical SRAM cell is shown in FIG. 1. The cell is made of a cross coupled inverter, each inverter having a pulldown transistor T1 or T2, a load p1 or p2, and a pair of transfer transistors T3, T4. The gate electrode of T1 is connected to the drain of T2, and the gate electrode of T2 is connected to the drain of T1 to provide the flip-flop operation. The load device pl, p2 may be a depletion or enhancement transistor or a high value resistor. The load devices pl and p2 are connected to the power supply V_{dd} on one side and to the drain of drive transistors T1, T2, respectively. The purpose of the resistor load pl, p2 and the power supply V_{dd} is to counteract the effect of charge leakage at the drains of the drive and transfer transistors (nodes N1 and N2). The gates of the transfer transistors T3, T4 are connected to a WORD line 8 and are switched ON by asserting the WORD line 8. The drain/source contacts of the transfer transistors are connected between the nodes N1, N2 and BIT lines 5, 6, respectively.

[0010] SRAM operation is well known. In brief, the charge (voltage) in nodes N1 and N2 represents the logic state of the cell. For example, to write a data of "1" in node N1, the bit line 5 is pre-charged to a desired voltage and the word line 8 is asserted. Node N1 is charged up and drives

N2 to a "no charge" or a low state. To read the cell, bit lines 5 and 6 are pre-charged and word line 8 is asserted. The bit line 6 is discharged through transistors T4 and T2 and the transient is sensed by a sense amplifier external to the cell.

[0011] A four transistor (4T) SRAM uses a high value resistor as its load device. The attraction of 4T SRAM is the potential for reduced cell size compared to a 6T SRAM (which uses transistors instead for load devices). The primary function of the load resistor is to supply enough current to compensate for the junction leakage and maintain the charge in the node. Junction leakage current typically ranges from femtoampere to picoampere ($l0^{-15}$ to 10 amps) for Field Effect Transistors (FET"s) fabricated under contamination free conditions, which is the minimum current required from the loaded (pl, p2) power supply V_{dd}. A typical maximum resistor value acceptable is in the range of $l0^{2}$ to $l0^{15}$ ohms, assuming a V_{dd} of 3 to 5 volts. The value of the resistor, in turn, is affected by availability of material that has very high intrinsic resistance and the cell area available for resistor layout. In addition, the resistor material and process should be compatible with silicon manufacturing.

[0012] Intrinsic polysilicon, a suitable material for high value resistors, can be used in a selected thickness range to provide sheet resistance as high as a few hundred gigaOhms, but it takes up a large part of the cell area. Since read operation causes temporary partial change in the charge stored in the nodes N1 and N2, a higher current from the loaded power supply can restore the charge in the nodes quickly to its "write value". This restoration may determine how fast data can be repeatedly read.

[0013] Softsusceptibility is increased when the charge in the node is off its maximum. Fast charging from the power supply can reduce soft error occurrence as the nodes will be charged to full voltage and, therefore, are less susceptible than if the charge levels were lower. Thus, considerations suggest use of a lower value leakage resistor.

[0014] However, the primary attraction of a 4T-SRAM continues to be its small size and lower manufacturing cost for stand alone memory. It has been the goal of many researchers to develop resistors of higher value so that a high value resistor can be easily integrated into the SRAM process using minimum chip area SRAMs which are susceptible to soft errors. A soft error occurs in an SRAM when ionizing radiation strikes the Si substrate and cre-

ates free electrons and holes. The free electrons and holes migrate under electric fields to different parts of devices, and can change the state of a memory cell or interfere with reading data from cells. Load resistor SRAMs may be more susceptible than 6Tif the current supply to restore soft error ionization is too small, i.e. on the order of picoampere per cell. However, use of high load current can lead to excessive power consumption. There is, therefore, a need to have an improved high resistance SRAM that requires a steady low current, is compatible with low power supplies, takes up very little space, has improved soft error tolerance and has low process complexity.

[0015] In a semiconductor chip environment in general, ESD protection is also important for shipment of semiconductor components. ESD protection may be provided by placement of ballasting resistors in series with MOSFETs in CMOS technology. Additionally, ESD protection is provided by placement of resistor elements in the emitter, base or collector in a bipolar transistor element. ESD is a concern in peripheral circuits, such as transmitter and receiver networks, system clocks, phase lock loops, capacitors, decoupling capacitors and fill shapes.

[0016] ESD events can occur from human body model (HBM)

events, machine model (MM) events, charged device model (CDM) events, and cable discharge events. These different events have different pulse widths and magnitudes, leading to different failure mechanisms. ESD failures can be prevented by placement of resistor elements in MOSFETs, bipolar transistors, or diode structures. Placement of the resistor elements in a MOSFET can be placed in the source, drain or gate region, and each will be influenced by different failure events. For example, gate structures of a MOSFET are sensitive to CDM events. Resistors in series with the drain structure assists HBM and MM events. In a bipolar transistor, placement of a resistor in series with the base is key to provide ESD protection of the Si bipolar junction transistor (BJT) device from HBM and MM events. Placement of resistors in the emitter also improves electrical and thermal stability. These elements must be placed not to impact the radio frequency (RF) characteristics of the semiconductor chip.

[0017] For example, ESD protection circuits for input nodes must also support quality DC, AC, and RF model capability in order to co-design ESD circuits for analog and RF circuits. With the growth of the high-speed data rate transmission, optical interconnect, wireless and wired marketplaces, the

breadth of applications and requirements is broad. Each type of application space has a wide range of power supply conditions, number of independent power domains, and circuit performance objectives.

[0018] Much effort has been expended by industry to address the problems described above. A difficulty in the design of prior art SER and RF ESD solutions to protect electronic devices from damage is that resistor elements introduce capacitive and inductive effects. They also require valuable space, resulting in reduced circuit design efficiencies. Hence, it is desirable to incorporate high quality resistive elements in semiconductor architectures that do not impact the RF performance of circuits yet provide ESD protection. It is desired to incorporate high quality resistive elements within transistor and similar gate structures that prevent single event induced latchup without reducing spacing efficiencies or adversely impacting circuit impedance, capacitance and parasitic resistance behavior.

SUMMARY OF INVENTION

[0019] The present invention provides a system and method for efficient resistor design for semiconductor circuit ESD, CMOS "latchup", electrical overstress (EOS), hot electron and soft error rate (SER) event protection. More particu-

larly, the present invention teaches an improved localized resistor placed in series with gate structures to prevent single event induced latchup and data loss. The invention also provides a system and method for efficient resistor design for ESD protection, wherein a resistor value or combination of resistor values is selected responsive to the transistor structure and ESD protection desired.

[0020] In one embodiment, ESD ballasting resistors are provided, wherein low value resistors are typically provided in series with MOSFET source or drain structures for HBM events. In another embodiment, high value resistors are used in series with a MOSFET gate. In another embodiment, ballasting in a Bipolar transistor is achieved with a low resistance element in series with the base, emitter or collector of an Si BJT or SiGe Heterojunction Bipolar Transistor (HBT) device.

[0021] The present invention provides an efficient low resistance high Q resistor element for ESD protection. The invention provides an efficient low value resistor for latchup reliability in a CMOS and BiCMOS technology, an efficient low value resistor for ESD reliability in a CMOS and BiCMOS technology; and an efficient high value resistor circuit for ESD reliability in a CMOS and BiCMOS technology.

Brief Description of Drawings

[0022] Figure 1 is a prior art SRAM circuit.

[0023] Figure 2 is a graphical image of a prior art MOSFET transistor structure.

[0024] Figure 3 is a graphical image of an Asymmetric MOSFET transistor structure with local resistor ballasting according to the present invention.

[0025] Figure 4 is a graphical image of an Asymmetric MOSFET transistor structure with local resistor ballasting interdigited into the contact structures according to the present invention.

[0026] Figure 5 is a graphical image of a Silicon-On-Insulator (SOI) Asymmetric MOSFET transistor structure with local resistor ballasting interdigitated into the contact structures and gate resistor structure according to the present invention.

[0027] Figure 6 is a graphical image of an SOI Asymmetric grounded gate MOSFET transistor structure with local resistor ballasting interdigited into the contact structures and gate resistor structure the guard ring structure for ESD according to the present invention.

[0028] Figure 7 is a schematic image of an Asymmetric grounded

gate MOSFET transistor structure with local resistor ballasting into the gate structure according to the present invention.

[0029] Figure 8 is a schematic diagram illustrating a grounded gate salicide blocked MOSFET structure and local resistor according to the present invention.

[0030] Figure 9 is a schematic diagram illustrating a drain ballasted salicide blocked MOSFET structure according to the present invention.

[0031] Figure 10 is a graphical layout illustrating a Silicon Germanium (SiGe) HBT device according to the present invention.

[0032] Figure 11 is a graphical layout illustrating an SiGe HBT device with local base resistor elements according to the present invention.

[0033] Figure 12 is a graphical layout illustrating an SiGe HBT device with local emitter resistor elements according to the present invention.

[0034] Figure 13 is a schematic diagram illustrating an SiGe HBT device with local emitter resistor elements according to the present invention.

[0035] Figure 14 is a cross section of an SiGe HBT device with the local resistor element integrated into the emitter structure

according to the present invention.

[0036] Figure 15 is a schematic diagram illustrating an SiGe HBT device with the local base resistor element according to the present invention.

[0037] Figure 16 is a cross section of an SiGe HBT device with the local resistor element integrated into the base structure according to the present invention.

[0038] Figure 17 is a graphical layout of an SOI lateral diode structure with local integrated resistor elements integrated with the gate structure according to the present invention.

[0039] Figure 18 is a cross section of an SOI lateral diode structure with local integrated resistor elements integrated with the gate structure according to the present invention.

[0040] Figure 19 is a schematic layout of an SOI lateral diode structure with local integrated resistor elements integrated with the gate structure according to the present invention.

[0041] Figure 20 is a top plan illustration of an SRAM cell showing localized resistor locations according to the present invention.

[0042] Figure 21 is a block illustration of a transistor contact according to the present invention.

[0043] Figures 22a through 22d illustrate another transistor structure according to the present invention.

[0044] Figure 23 is a detail illustration of an interface of an M1, silicon resistor film layer and contact of an SRAM according to the present invention.

[0045] Figure 24 is a graphical illustration of 4-point resistance measurements of three SRAM wafer embodiments of the present invention.

[0046] Figure 25 is a graphical illustration of 2-point resistance measurements as a function of applied voltage of the three embodiments of Figure 24.

Detailed Description

[0047] Referring now to Figure 2, a graphical image of a standard prior art MOSFET transistor structure 200 is provided. MOSFETs are vulnerable to ESD events. ESD damage is evident in the source and drain diffusions and gate structure. Non-uniform current constriction also leads to early failure. In order to provide ESD and latchup protection, the MOSFET 200 contains source 202, drain 204 and gate structure 206 separated by large Salicide block mask "OP"resistor structures 210. However, in order to fit the block mask resistor structures 210 into the prior art MOSFET 200, the widths of the diffusions underneath must be

expanded. Therefore, the spacing 212 between the gate 206 and the drain 204 contacts 220, and the spacing 242 between the gate 206 and the source 202 contacts 244 must be accordingly enlarged to accommodate the block mask resistor 210 structures, thus resulting in additional capacitance and large inefficiencies of area, spacing, materials and overall device size.

[0048] Figure 3 is a graphical image of an Asymmetric MOSFET transistor structure 300 with local resistor ballasting according to the present invention. It is Asymmetric in that the drain 304 resistance is not equal to the source 302 resistance. An advantage of the present invention is that adding a local resistor element Asymmetrically introduces resistor ballasting effects in the drain structure 304 without requiring corresponding resistor structures on the source side 302 or either OP block 310. Through resistor ballasting, the RF ESD benefits of a high-resistance structure under prior art techniques can be accomplished with a medium or low resistance structure. A one to 100 Ohm local resistor structure can thus accomplish the ESD benefits equivalent to a mega-Ohm large resistor incorporated into the structure through prior art techniques. Using a small resistor on the order of the contact hole size re-

duces capacitive and inductive effects. Other solutions such as diffused resistors or even wire interconnects are area intensive and lead to poor Q values due to inductive and capacitive effects. Using the local resistor 320, good ESD ballasting is achieved without RF degradation effects.

[0049] Figure 4 is a graphical image of another Asymmetric MOS-FET transistor structure 400 according to the present invention with local resistor 422 ballasting interdigited into the contact structures 420. Adding a local resistor element 422 introduces ballasting in the drain structure 404. Here the local resistor ballasting provides satisfactory ESD and latchup protection, obviating the need for salicide block mask structures. Using a small resistor 422 on the order of the contact hole size reduces capacitive and inductive effects. Other solutions such as diffused resistors or even wire interconnects are area intensive and lead to poor Q values due to inductive and capacitive effects. Using the local resistor 422, an advantage is that good ESD ballasting is achieved without RF degradation effects. Additionally, by choosing the location of the contact 444 relative to the resistor 422, non-uniform thermal distribution can be compensated and improved lateral current distribution is achieved.

[0050] Figure 5 is a graphical image of a Silicon-on-insulator (SOI) Asymmetric MOSFET transistor structure 500 according to the present invention with local resistor ballasting interdigited into the contact structures 502 and 504 and gate resistor structure 520. Adding a local resistor element 504 introduces ballasting in the drain structure 510. Using a small resistor 504 on the order of the contact hole size reduces capacitive and inductive effects. Other solutions such as diffused resistors or even wire interconnects are area intensive and lead to poor Q values due to inductive and capacitive effects. Using the local resistor 504, good ESD ballasting is achieved without RF degradation effects. In SOI technology, failure mechanisms unique to SOI occur between the gate 520 and the drain 510, and the gate 520 and the source 530. Hence, in SOI having a high resistance element in series with the gate can eliminate Charge Device Model failure mechanisms observed in advanced SOI microprocessors.

[0051] An important advantage of the present invention illustrated in Figure 5 is that the local resistor may be selectively introduced into a specified number of contact regions responsive to the current flow modification desired. As illustrated, three local resistors 504 are introduced into

three specified contact regions 502 in the drain region 510, into an alternating arrangement with drain contacts 504. Thus, the present invention enables the introduction of non-uniform resistance on one side only of the source-drain structure. This enables spreading out current flow, or optimizing current flow, on the drain side by the selective placement of the local resistors 504. This is very important in high current flow applications, because current flow through a transistor source-drain structure is not uniform. The present invention enables modulation of that current flow through the selective placement of the local resistors 504.

[0052] The ballasting local resistors discussed thus far are formed within contact holes within transistor drain structures. Where the structural dimensions available to the local resistors are limited to the size of contact holes under the present invention, their resistance values are also necessarily limited by this physical constraint. Generally, the drain contact hole local resistors resistance values cannot provide mega-Ohm values, which some applications may demand.

[0053] Figure 6 is a graphical image of an Asymmetric MOSFET transistor structure 600 according to the present inven-

tion with local resistor ballasting in the drain and gate structures. As discussed above, adding a contact local resistor element 604 introduces ballasting in the drain structure 610. Using a small resistor on the order of the contact hole size 602 reduces capacitive and inductive effects. Other solutions such as diffused resistors or even wire interconnects are area intensive and lead to poor Q values due to inductive and capacitive effects. Using one or more drain contact local resistors 604 provides good ESD ballasting without RF degradation effects. Another advantage of the present invention is the addition of a local resistor 650 to the gate 620. This local resistor 650 cuts back the current flow through the gate structure 620, which improves the current leakage characteristics of the gate 620. Placing the local resistance 650 in series with the gate 620 also improves the impedance of the gate structure 620 and thereby improves ESD protection for the MOSFET 600.

[0054] Figure 7 is a schematic image of an Asymmetric grounded gate MOSFET transistor structure 700 with local resistor 750 ballasting in the gate structure 720. In this structure, the gate 720 is OFF and "tied" to ground 760. It is important that the gate 720 is not hardwired directly to ground,

but is instead "coupled" to ground 760 through the local resistor 750 placement in the gate contact hole 752. When the gate 720 is grounded in this fashion, the impedance is still significant between the gate 720 and the true source 730 contact point. The gate 720 structure can now re-spond from an ESD pulse associated with the RC response of the high resistance and native capacitance of the drain 710. Hence, the gate structure 720 will couple to an input source contact pad 744 when an ESD event occurs. This advantage is key to ESD protection of this circuit. Using the gate local resistor 750 good ESD ballasting is achieved without RF degradation effects.

[0055] It is preferable that a high resistance resistor 750 is pro-vided in the gate structure 720. Using a low resistance contact resistor in the drain, and a high resistance in the gate structure, current will flow from source to drain with-out limitations. Additionally, the gate structure can now respond from the ESD pulse associated with the RC re-sponse of the high resistance and native capacitance of the drain. Hence, the gate structure will couple to the in-put pad when an ESD event occurs. This advantage is key to ESD protection of this circuit. Also, in a CDM event a charge comes into a prior art MOSFET device substrate

through a source 630 and passes through the gate and then back into the drain avoiding the source: in the present embodiment the impedance provided by the local resistor 750 in series with the gate 720 will avoid that current path. These advantages are also provided with an economy of size due to the placement of the resistor 752 within the contact hole 752.

[0056] Figure 8 is a schematic diagram illustrating a grounded gate salicide blocked MOSFET structure 800 coupled to a ground 810. Adding salicide block masks to achieve ESD ballasting requires area and adds extra loading effect due to the source and drain capacitance. This technique integrates the local gate resistor 802 into the MOSFET, but is limited by the source/drain resistance values of the implants.

[0057] Figure 9 is a schematic diagram illustrating a salicide blocked MOSFET structure and local resistor ballast elements coupled to a ground 910 according to the present invention.To provide drain effects, a drain resistor 952is used in series with the drain 910, source 930 and gate 920 with local gate resistor 950 structure. Because higher resistor values can have an adverse impact and slow down device performance, a medium resistance value local re-

sistor 950 of from about 10 to about 100 Ohms is typically preferred for this application. For example, a 10 Ohm driver trying to drive the local resistor 950 in series with a receiver is looking for certain impedances, and a medium range resistor will provide superior performance over a high range resistor typically found in prior art ESD structures. Adding salicide block masks to achieve ESD ballasting requires area and adds extra loading effect due to the source and drain capacitance. This standard technique integrates the resistor into the MOSFET but is limited to the source/drain resistance values of the implants. Adding the local resistor does not impact the Q of the RF element nor area. By providing both solutions, the resistance of the drain and source is not dependent on the MOSFET source drain series sheet resistance.

[0058] Figure 10 is a graphical layout illustrating a typical prior art Silicon Germanium Transistor (SiGe) 1000. Contacts 1008 are formed within emitter 1006, base 1004 and collector 1002 regions. For ESD protection issues, the SiGe transistor is vulnerable to emitter 1006, base 1004 and collector 1002 failure mechanisms. Common weaknesses of this element are base 1004-emitter 1006 failure mechanisms. Failures also occur at the collector 1002 to emit-

ter 1006 interface.

[0059] Figure 11 is a graphical layout illustrating an SiGe transistor 1100 with local resistor elements 1102 incorporated into selected contact regions 1110 within the base 1124 according to the present invention. The local resistor elements 1102 provide ESD protection from base 1124-emitter 1126 failure mechanisms. SiGe HBT devices require high frequency operation and are impacted by inductive and capacitive resistor elements. Hence, having a resistor 1102 local to the device which does not add capacitance or inductance has an advantage. The resistor 1102 changes the effective base resistance of the base 1104, and thereby provides ESD protection. Additionally, by selectively choosing and locating resistors in some base contact holes 1110 and not locating resistors in other base contact holes 1130, the present invention can also be used to modulate lateral resistor ballasting issues in the base lateral to the current flow.

[0060] Figure 12 is a graphical layout illustrating an SiGe transistor 1200 with local emitter 1202 resistor elements 1204 incorporated into emitter contacts 1210 according to the present invention. Contact regions 1228 are formed within emitter 1202, base 1206 and collector 1216 re-

gions. SiGe HBT devices require high frequency operation and are impacted by inductive and capacitive resistor elements. Hence, having a resistor 1204 local to the device which does not add capacitance or inductance has an advantage. The emitter resistor 1204 can provide ESD protection as well as can be used to modulate lateral resistor ballasting issues in the base 1206 lateral to the current flow. Emitter ballasting provides both electrical and thermal stability.

[0061] Because of loading effects and frequency response, a low resistance value is preferred in the emitter resistor 1204 to minimize performance impact. Thus, a "high Q"element is preferred. There should be no parasitic resistance, conductance or capacitance affiliated with the use of the local resistor 1204. Building a resistor out of silicon materials typically results in silicon capacitance, inductance or space issues. Therefore, a significant advantage of the present invention for SiGe structures is the ability to provide a small, compact resistor element within the contact holes that does not have the inherent disadvantages of resistor elements fabricated from the Si structural elements, such as the large salicide block mask "OP"resistor structures 210 of Figure 2. Emitter local resistor 1204 re-

sistance values on the order of about one to about ten Ohms will provide good emitter ballasting. The limited resistance values also provide thermal and electrical stability advantages over prior art device resistor structures.

[0062] Figure 13 is a schematic diagram illustrating an SiGe transistor local emitter resistor circuit 1300. The SiGe transistor 1304 and local emitter resistor element 1310 are integrated into output stage solution 1320, which results in improved performance and a savings of about 30% area over a prior art structure that uses an external resistor (not shown). SiGe HBT devices require high frequency operation and are impacted by inductive and capacitive resistor elements. Hence, having a resistor 1310 local to the device which does not add capacitance or inductance has an advantage. The emitter resistor 1310 can provide ESD protection as well as can be used to modulate lateral resistor ballasting issues in the base lateral to the current flow. Emitter ballasting provides both electrical and thermal stability. A low resistance value is preferred to minimize performance impact. Resistance values on the order of about one to about ten Ohms will provide good emitter ballasting according to the present invention.

[0063] Figure 14 is a cross section of an SiGe transistor 1400

with a local resistor element 1410 integrated into the contact hole 1412 of the emitter structure 1420 according to the present invention. An emitter region 1421 projects into the contact hole 1412; the hole 1412 formed as an opening in a dielectric substrate material 1415. A conductive metal layer 1411 is disposed over the dielectric substrate 1415, with conductive element 1413 forming a structural and circuit connection between the metal layer 1411 and the local resistor 1410. The emitter resistor 1410 can provide ESD protection as well as can be used to modulate lateral resistor ballasting issues in the base 1422 lateral to the current flow. The device incorporates an external resistor element 1432, and internal resistor element 1426 and a resistor link structure 1428. STI region 1430 and P+ region 1424 portions are also shown. Emitter ballasting provides both electrical and thermal stability. A low resistance value is required to minimize performance impact. Resistance values on the order of about one to about ten Ohms will provide good emitter ballasting. This structure thus provides improved performance for transistors running at speeds of 45, 90, 200 and 300 Gigahertz.

[0064] Figure 15 is a schematic diagram illustrating an SiGe tran-

sistor 1500 with a local base resistor element 1510 wherein the base 1516 is coupled to ground 1520. A weakness of an SiGe transistor is the base-emitter failure mechanisms. SiGe HBT devices require high frequency operation and are impacted by inductive and capacitive resistor elements. Hence, having a resistor 1510 local to the device which does not add capacitance or inductance has an advantage, as well as providing an area savings of about 20% over external resistor structures (not shown). The base resistor 1510 can provide ESD protection as well as can be used to modulate lateral resistor ballasting issues in the base lateral to the current flow.

[0065] Figure 16 is a cross section of an SiGe transistor circuit 1600 with a local resistor element 1610 integrated into two parallel base structures 1620 according to the present invention. An N-Collector 1630 is bordered by P+ regions 1636 and STI regions 1634, and above an N+ pedestal 1638 and an N++ subcollector 1640. An N+ emitter 1632 is disposed above the collector 1630. Base projections 1620, conductive elements 1646 and local resistors 1610 are located within contact holes 1645; the holes 1645 formed as openings in a dielectric substrate material 1644. The conductive elements 1646 form structural and

circuit connections between metal layers 1642 and the local resistors 1610. A weakness of an SiGe transistor is the base 1620-emitter 1632 failure mechanisms. SiGe HBT devices require high frequency operation and are impacted by inductive and capacitive resistor elements. Hence, having a resistor local to the device which does not add capacitance or inductance has an advantage. The base resistor 1610 can provide ESD protection as well as can be used to modulate lateral resistor ballasting issues in the base 1620 lateral to the current flow. The circuit 1600 may be grounded, or it may be an input circuit without grounding.

[0066] Figure 17 is a graphical layout of a Silicon-on-insulator (SOI) lateral diode circuit 1700 with a local integrated resistor element 1710 integrated into the gate structure 1720 according to the present invention. In SOI technology, lateral elements are used for ESD protection. The SOI lateral diode 1700 differs from a transistor structure. One side is a "PFET-type"structure 1730, and the other is an "NFET-type"structure 1740. A mask 1750 is dropped down the middle, with the gate 1720 "P-doped"on one side 1722 and "N-doped"on the other side 1724. Thus, the lateral diode 1700 does not define an npn or pnp

structure like a transistor. Instead, it may be a p+p-n+ or p+p-n- device, dependent upon the doping of the gate 1720. Using a local resistor element 1702 in the anode 1730, cathode 1740 or gate 1720 regionallows prevention of failure during ESD events. CDM failures in prior art structures typically occur through the gate structure 1720 from gate-to-source and gate-to-drain. Adding a resistor1710 to the gate structure 1720 prevents electrical overstress of the gate structure from HBM, MM and CDM events. In receiver networks, SOI failures occurred through pass transistors leading to failure. Having the local resistor structures 1702 and 1710 in the contact holes prevents ESD failures in SOI microprocessors.

[0067] Figure 18 is a cross section of an SOI lateral diode structure 1800 with local integrated resistor element 1802 integrated within the gate structure 1810 according to the present invention. The device 1800 is a Lubistor with an abrupt junction. An N+ cathode 1840 and P+ anode 1830 are provided about a gate structure 1810. The gate structure 1810 includes a mask 1817, one side of which is an N+-doped region 1811, the other side being a P+ doped region 1813, with these structures disposed above an N- region 1815. STI regions 1812, a buried oxide layer 1814

and a P-/P+ substrate 1816 are also provided. A conductive metal layer 1822 is in circuit connection with the local resistor 1802. Although the present embodiment illustrates local resistor elements 1802 in all of the anode 1830, cathode 1840 and gate 1810 regions, the local resistor may be allocated in only one or more of these regions 1830, 1840 and 1810. Using a local resistor element 1802 in the anode 1830, cathode 1840 or gate region 1810 allows prevention of failure during ESD events. CDM failures occur through the gate structure from gate to source, and gate to drain. Adding a resistor 1802 to the gate structure 1810 prevents electrical overstress of the gate structure 1810 from HBM, MM and CDM events. In receiver networks, SOI failures occurred through pass transistors leading to failure. Having the local resistor structure 1802 in the contact hole prevents ESD failures in SOI microprocessors. This element is key to providing success in SOI technology.

[0068] Figure 19 is a schematic layout of an SOI lateral diode circuit 1900 according to the present invention. A polysilicon bound diode 1904 with a gate structure 1920 is parallel to a local integrated resistor element 1902. Using a local resistor element 1902 in the gate region 1920 allows pre-

vention of failure during ESD events. CDM failures occur through the gate structure from gate to source, and gate to drain. Adding a resistor 1902 to the gate structure prevents electrical overstress of the gate structure from HBM, MM and CDM events. In receiver networks, SOI failures occurred through pass transistors leading to failure. Having the local resistor structure in the contact hole prevents ESD failures in SOI microprocessors.

[0069] What is important is that the present invention teaches the use of localized resistor elements that keep the Q factor high and resistance up enough to drive current through the circuit and thereby enable use of the circuit through current flow when the circuit is in use, and to provide protection to stop current flow through the circuit from latchup, HBM, MM and CDM events when the circuit is not in use. As illustrated above, the present invention may be applied in SOI and CMOS applications, as well as MOSFET circuitry, by integrating with SiGe transistors.

[0070] With respect to the prevention of soft-error latch upsets in SRAM applications, as described above, it is desirable to insert a resistance in the path of a cross coupling structure. It is also preferred to do so without increasing the size of the cell. Figure 20 illustrates a typical SRAM cell

layout showing the location of the nodes 2002 and 2004 and proposed locations of localized resistors 2003 and 2005 according to the present invention.

[0071] Figure 21 is a block illustration of a W CA transistor contact 2104 illustrating preferred locations 2106 and 2108 for a localized resistor film according to the present invention. A polysilicon gate node 2112 is disposed above oxide 2116, pfet 2122 and nfet 2124 regions. By adding a resistor film 2130 between an M1 metal layer 2110 and a polysilicon gate node 2112 in a cross coupling node region 2101, at either a contact-to-MI interface 2106 or a contact-to-polysilicon gate interface 2108, and limiting the width of the resistance film 2130 to the width of the contact via hole 2120, a localized resistor 2130 may thus be added without increasing the cell size.

[0072] The actual size and alignment of the localized resistor film 2130 is critical to the invention because the electrical characteristics of the resultant contact 2104-resistor film 2130 circuit will be determined by the material properties, area and size of the contact 2104. Is preferred that the localized resistor film 2130 is an insulating or semi-insulating material. Suitable materials include a tunnel oxide or nitride, silicon-implanted oxide or nitride. Ap-

propriate values and resistance are determined by SER immunity and by the write speed and functionality of the device 2101. Typically low resistance excursions are not a problem with the present invention. In fact, a few cells may be more susceptible to SER.

[0073] In one embodiment of the invention, a transistor structure is formed as follows. All transistor structures are defined and formed in a typical prior art manner, up to and including contact fill and polish. A local resistor film according to the present invention is then deposited upon the contact. A suitable film may be an amorphous polysilicon, 0.1 microns thick, 100 O-cm. A mask is applied and the resistance film is removed from all but relevant contacts. Normal processing then proceeds to a standard M1 etch, with the M1 etch stopping on the film. Normal processing then proceeds again.

[0074] In another embodiment of the present invention, a transistor device is defined through typical prior art process steps, up to the step of depositing a barrier nitride film. A resistor film is then deposited; processing then continues as usual up to the "contact etch" step. All contacts are etched through the barrier nitride, with etching stopping on the new resistor film. Mask and etching steps than

proceed, with the resistance film being etched away from all but relevant contacts. Normal device processing then proceeds again.

[0075] In another embodiment of the present invention, transistor devices are again defined in a typical prior art manner up to an M1 insulator deposition step. M1 troughs are defined for resistive contact formation. A resistor film, such as an amorphous polysilicon, 0.1 microns thick, 100 O-cm, is deposited in the defined troughs. Additional desired M1 troughs are then defined, and typical device processing steps then proceed from this point to complete the manufacture of the device.

[0076] Embodiments described above provide high resistance, local resistor-contact structures without changing cell size. The present invention also teaches methods and structures using processes and materials and is compatible with copper integration schemes.

[0077] Figures 22a through 22d illustrate another transistor structure according to the present invention. Figure 22a shows a conventional transistor structure 2200 manufactured up to the point of an M1 etch step, wherein contacts 2210 are formed within vias 2212. A dielectric substrate 2214 is formed on the upper surface 2215 of the struc-

ture 2200, and vias 2216 are formed above the contacts 2210.

[0078] In Figure 22b, a silicon layer 2220 is then sputter deposited onto the exposed dialectic substrate surfaces 2217 and the upper surfaces 2219 of the contacts 2210. Figure 22c illustrates the step of treating 2230 the silicon layer 2220, such as with an Ozone process or an air exposure process. In order to minimize the oxide consumption when in contact with the metal barrier (TaN/Ta), it is preferred that a second silicon layer (not shown) is deposited onto the silicon layer 2220 and treated in a similar fashion. The structure 2200 is then processed for the remaining M1 etch through typical prior steps; liner seed, plating, and then CMP are completed. The resulting structure as illustrated in Figure 22d provides high resistance contact structures formed by the contact 2240 and silicon resistor film layer 2221 on the nodes 2250 of the SRAM cell 2260 to protect against SER"s according to the present invention.

[0079] Figure 23 is a detail illustration of an interface 2265 of the M1 2240, silicon resistor film layer 2221 and contact 2210 of an SRAM 2260 according to the present invention.

[0080] Figures 24 and 25 provide graphical illustration of the behavior of three SRAM wafer embodiments of the present invention: "EXAMPLE 1"2402, "Example 2"2406 and "Example 3"2410. Example 1 is an SRAM wafer wherein a first resistive layer comprising 200 angstroms (A) Si is sputter disposed in a first chemical vapor deposition step upon an upper surface including a contact stud. The sputter tool apparatus then admits air for a "momentary air exposure break"for anywhere from about one minute to about ten minutes in a minimal oxidation second step, wherein the Si layer reacts with the air to form a silicon nitride compound layer. In a third step, the sputter tool then disposes another 200 A Si layer on top of the silicon nitride compound layer. Thus Example 1 provides an $Si/Si_xN_yO_z$ local resistor layer structure, where x, y and z are the atom numbers.

[0081] Example 2 and Example 3 are two other SRAM wafers wherein a first resistive layer comprising 200 A Si is sputter disposed in a first chemical vapor deposition step upon an upper surface including a contact stud. Ozone is then used in a minimal oxidation second step. Ozone is more reactive than air and is preferred over air to allow for improved control of oxidizing gas flow and the film

thicknesses of the resultant oxidized layer. Accordingly, the time of oxidizing gas exposure is typically much shorter than the times required for air exposure as in the process for EXAMPLE 1, with Ozone gas exposure times preferably on the order of seconds or single digit minutes. The Si layer reacts with the Ozone to form a Silicon oxide compound layer. In one embodiment, the resultant Si_xO_y layer has a thickness of about 180 A, where x and y are the atom numbers. In a third step, the sputter tool then disposes another 200 A Si layer on top of the silicon oxide compound layer. Thus, Example 2 and Example 3 provide an Si/Si_xO_y local resistor layer structure.

[0082] Figure 24 illustrates 4-point isolated CA resistance measurements at 1uA, and Figure 25 illustrates 2-point median isolated CA resistance as a function of voltage, for each of EXAMPLE 1 2402, Example 2 2406 and Example 3 2410.

[0083] Figures 26 is a sectional illustration of another SRAM wafer according to the present invention. A copper M1 layer 2602 forms a circuit with a contact 2606 through a local resistor Si film layer 2610, wherein the copper layer 2602 and local resistor 2610 are formed within a void 2605 within a silk material 2604. The contact 2606 is

formed within a bpsg material 2612. Figure 27 plots the resistance behavior of two embodiments of the resistor layer 2610 as on three different examples wherein 50 chips per wafer are tested.For a typical prior art process-of-record (POR) structure 2702, with a prior art M1-to-contact structure without a resistive layer, the resistance values 2703 are all less than about 5 Ohms. For an M1-to-contact structure 2704 incorporating a 35 A thick Si layer 2610 according to the present invention, the resistance values 2705 reflect around 50 or less Ohms, thus providing a medium resistance local resistor structure preferable in some of the embodiments of the invention described above. And for an M1-to-contact structure 2706 incorporating a 50 A thick Si layer 2610, the resistance values 2707 reflect between about 100 to about 500 Ohms, thus providing a higher range of medium resistance local resistor structures preferable in some of the embodiments of the invention described above.

[0084] Figure 28 illustrates the resistance values returned by first and second embodiments 2802 and 2810, respectively, of Si local resistor films according to the present invention, wherein embodiment 2810 is produced through the process utilized to produce embodiment 2802, with the addi-

tional step of incorporating a Boron dopant. As reflected in the graph, the Boron doping process step reduces resistance values; however, the resultant local resistor structure values range greatly. Thus, embodiment 2810 may be preferable where some but not all of the contact studs require lower resistance, and especially where lateral ballasting issues prefer a non-uniform resistance distribution among the contact studs incorporating the local resistor film.While the invention has been described in terms of a single preferred embodiment, various alternatives and modifications can be devised by those skilled in the art without departing from the invention. Accordingly, the present invention is intended to embrace all such alternatives which fall within the scope of the appended claims.